



PATENTS
174/183
(A568)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicants : Edward Aung et al.
Application No. : 09/805,843 Confirmation No.: 3795
Filed : March 13, 2001
For : CLOCK DATA RECOVERY CIRCUITRY ASSOCIATED
WITH PROGRAMMABLE LOGIC DEVICE CIRCUITRY
Art Unit : 2638
Examiner : Emmanuel Bayard

New York, New York 10020
March 7, 2006

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, applicants
hereby make the following documents of record in the above-
identified patent application:

U.S. PATENT DOCUMENTS

4,229,825	Guidoux	10/21/1980
4,680,779	Wakerly	07/14/1987
5,034,967	Cox et al.	07/23/1991
5,084,891	Ariyavisitakul et al.	01/28/1992
5,162,762	Flanagan	11/10/1992
5,184,350	Dara	02/02/1993
5,357,249	Azaren et al.	10/18/1994

U.S. PATENT DOCUMENTS

5,457,717	Bellamy	10/10/1995
5,481,563	Hamre	02/02/1996
5,483,180	Chai et al.	01/09/1996
5,552,942	Ziperovich et al.	09/03/1996
5,757,240	Boerstler et al.	05/26/1998
5,781,038	Ramamurthy et al.	07/14/1998
5,793,822	Anderson et al.	08/11/1998
5,838,749	Casper et al.	11/17/1998
5,963,608	Casper et al.	10/05/1999
5,999,025	New	12/07/1999
6,031,473	Kubinec	02/29/2000
6,178,213 B1	McCormack et al.	01/23/2001
6,256,722 B1	Acton et al.	07/03/2001
6,266,799 B1	Lee et al.	07/24/2001
6,295,563 B1	Whittaker	09/25/2001
6,327,196 B1	Mullarkey	12/04/2001
6,341,142 B2	Ducaroir et al.	01/22/2002
6,421,796 B1	Gatherer	07/16/2002
6,463,109 B1	McCormack et al.	10/08/2002
6,538,656 B1	Cheung et al.	03/25/2003
6,631,144 B1	Johansen	10/07/2003
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6,834,367 B2	Bonneau et al.	12/21/2004
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JP 04287439 A	Japan	10/13/1992
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OTHER DOCUMENTS

Charles R. Hogge, Jr., "A Self Correcting Clock Recovery Circuit," IEEE Transactions On Electron Devices, Vol. ED-32, No. 12, pp. 2704-2706, December 1985.

Timothy H. Hu et al., "A Monolithic 480 Mb/s parallel AGC/Decision/Clock-Recovery Circuit in 1.2- μ m CMOS," IEEE Journal Of Solid-State Circuits, Vol. 28, No. 12, December 1993.

Ilya I. Novof et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ± 50 ps Jitter," IEEE Journal Of Solid-State Circuits, Vol. 30, No. 11, pp. 1259-1266, November 1995.

Ricardo Monleone, "Clock-recovery PLL fits into single PLD," EDN, pp. 88-92, November 23, 1995.

Fong, Thomas Kin Tak, "Advanced clock recovery techniques for high-speed packet-switched optical networks," ProQuest, Abstract (Document Summary), 1995.

M. Rau, et al., "Clock/Data Recovery PLL Using Half-Frequency Clock," IEEE Journal Of Solid-State Circuits, Vol. 32, No. 7, July 1997.

German Gutierrez et al., "Unaided 2.5 Gb/s Silicon Bipolar Clock and Data Recovery IC," IEEE Radio Frequency Integrated Circuits Symposium, VIII-7, pp. 173-176, 1998.

Ankit Seedher et al., "Fractional Rate Phase Detectors for Clock and Data Recovery," IEEE, pp. 313-316, 2003.

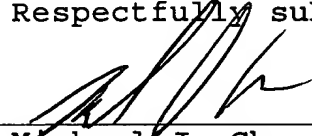
The aforementioned U.S. Patent Documents, which are listed on the accompanying Form PTO/SB/08A (submitted in duplicate), fall under 37 C.F.R. § 1.98(a)(2)(ii) for which documents the requirement to provide copies is waived. Accordingly, no copies of the aforementioned U.S. Patent Documents are provided. Copies of the "Foreign Documents" and "Other Documents" are enclosed herewith.

It is respectfully requested that the aforementioned documents be (1) fully considered by the U.S. Patent and Trademark Office during the examination of this application; and (2) printed on any patent which may issue on this application. Applicants request that a copy of the enclosed

Form PTO/SB/08A, as considered and initialed by the Examiner,
be returned with the next communication.

An early and favorable action is respectfully
requested.

Respectfully submitted,



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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 3



Application Number	09/805,843
Filing Date	March 13, 2001
First Named Inventor	Edward Aung
Art Unit	2638
Examiner Name	Emmanuel Bayard
Attorney Docket Number	174/183
Confirmation Number	3795

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		4,229,825	10/21/1980	Guidoux	
		4,680,779	07/14/1987	Wakerly	
		5,034,967	07/23/1991	Cox et al.	
		5,084,891	01/28/1992	Ariyavisitakul et al.	
		5,162,762	11/10/1992	Flanagan	
		5,184,350	02/02/1993	Dara	
		5,357,249	10/18/1994	Azaren et al.	
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		5,781,038	07/14/1998	Ramamurthy et al.	
		5,793,822	08/11/1998	Anderson et al.	
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		5,999,025	12/07/1999	New	
		6,031,473	02/29/2000	Kubinec	
		6,178,213 B1	01/23/2001	McCormack et al.	
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		6,266,799 B1	07/24/2001	Lee et al.	
		6,295,563 B1	09/25/2001	Whittaker	

Examiner
SignatureDate
Considered

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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		6,421,796 B1	07/16/2002	Gatherer	
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		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
		JP 04287439 A	10/13/1992	Fujitsu Ltd.		
		JP 05199107 A	08/06/1993	Hitachi Ltd Hitachi Comput Eng Corp. Ltd.		
		JP 08032569 A	02/02/1996	NEC Eng Ltd.		
		GB 2 011 764 A	07/11/1979	Telecommunications Radioelectriques Et Telephoniques T.R.T.		

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NON PATENT LITERATURE DOCUMENTS

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		Charles R. Hogge, Jr., "A Self Correcting Clock Recovery Circuit," IEEE Transactions On Electron Devices, Vol. ED-32, No. 12, pp. 2704-2706, December 1985.
		Timothy H. Hu et al., "A Monolithic 480 Mb/s parallel AGC/Decision/Clock-Recovery Circuit in 1.2- μ m CMOS," IEEE Journal Of Solid-State Circuits, Vol. 28, No. 12, December 1993.
		Ilya I. Novof et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ± 50 ps Jitter," IEEE Journal Of Solid-State Circuits, Vol. 30, No. 11, pp. 1259-1266, November 1995.
		Ricardo Monleone, "Clock-recovery PLL fits into single PLD," EDN, pp. 88-92, November 23, 1995.
		Fong, Thomas Kin Tak, "Advanced clock recovery techniques for high-speed packet-switched optical networks," ProQuest, Abstract (Document Summary), 1995.
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		German Gutierrez et al., "Unaided 2.5 Gb/s Silicon Bipolar Clock and Data Recovery IC," IEEE Radio Frequency Integrated Circuits Symposium, VIII-7, pp. 173-176, 1998.
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